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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/953,719	10/17/1997	DAISUKE YOSHIDA	35.C12338	4164

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EXAMINER
PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 12/06/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 08/953,719	Applicant(s) YOSHIDA ET AL.	
	Examiner Jeff Piziali	Art Unit 2673	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 09 November 2001 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 5 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed amendment(s) will not be entered because:

   (a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1,2,4,5,7-19,21,22 and 24-48*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☒ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). *20*.

10. ☒ Other: *See Continuation Sheet*

AP 12/3/01

Continuation of 2. NOTE: The proposed amendments to independent claims 18, 38 and 43 incorporate the newly added limitation of "a buffer disposed between said D/A converter and said plural signal transfer switches, which stores the analog signal of inverted polarity from the D/A converter." Although this same limitation was previously incorporated into independent claim 1, until now, the limitation has remained separate and foreign from all other independent claims. Adding this limitation to independent claims 18, 38 and 43 would result in the creation of hitherto unseen inventive combinations. Such combinations would constitute new issues, requiring further consideration.

Continuation of 10. Other: The applicants contend, regarding claim 1, that the combination of Lewis (5,589,847) and Yamaguchi (5,438,342) fails to teach signal inversion prior to or in concert with a D/A converter, and instead "requires the signal inversion technique to occur after the D/A converter, allowing for signal decay and introduction of noise" (see Paper No. 19, Page 6, 2nd Paragraph). However, the examiner respectfully notes that claim 1 recites circuitry "which inverts the polarity of the analog signal from the D/A converter" (see Lines 19-22). As the pending claim reads, signal inversion does indeed occur after analog conversion.

The applicants further contend that incorporating the inversion technique of Yamaguchi would render a combination of Lewis, Yamaguchi and Shinya (5,170,158) inoperable. The examiner respectfully disagrees. Lewis teaches every limitation found in claim 1, except signal inversion and buffering. Although both signal inversion and buffering are (and were at the time of invention) well known and commonly utilized to respectively limit flicker/crosstalk and synchronize/level signal output; the examiner has chosen to provide specific prior art references and illustrations of such circuitry and techniques. Yamaguchi plainly teaches a standard manner of analog image signal inversion (see Column 2, Lines 1-29); and Shinya clearly illustrates the buffering of DAC image signals (see Fig. 2). Although Lewis, Yamaguchi and Shinya all disclose distinct and unique display devices; the beneficial implications of polarity inversion and signal buffering are common to all three inventions. There is nothing in the prior art that would lead an artisan to the conclusion that such polarity inversion and signal buffering would render Lewis' display device inoperable.

The applicants point out the distinct and unique driving techniques provided by Shinya and Yamaguchi. However, these references were not provided by the examiner as examples of driving techniques. They were (and remain) intended to serve as prior art examples of polarity inversion and analog buffering.

Finally, the applicants argue the prior art does not even suggest the desirability of combining Yamaguchi's polarity inversion technique and Shinya's output buffers to Lewis' display driving circuitry. However, the applicants do admit that Yamaguchi discloses polarity inversion "as suppressing flicker and crosstalk to some extent" (see Paper No. 19, Page 8, 2nd Paragraph). While Yamauchi does attempt to improve upon the background art shown in Fig. 1, the desirability of polarity inversion is still established just the same. Because Yamaguchi thinks he's stumbled upon an improved driving technique, doesn't mean the benefits of the conventional method have suddenly been invalidated. To see proof, one need look no further than the applicant's own pending invention.

Under such reasoning, the rejection of the claims is deemed proper and thereby maintained.

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